Name: Dr. Stelios Neophytou

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University of Nicosia
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Nicosia, Cyprus.

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Personal: **Birthday:** 11 Aug. 1978

Education: **Undergraduate work:** Engineering Diploma from Computer Engineering and Informatics Department, University of Patras, Greece. ***Grade***: 8.80 (distinction), July 2003.

Graduate work: PhD in Computer Engineering from Electrical and Computer Engineering Department, University of Cyprus, May 2009.

Positions Held:

Feb. 2013- present:	Assistant Professor at University of Nicosia.
Jan. 2009 – Jan 2013:	Lecturer at University of Nicosia
Fall semester 2008:	Special Teaching Staff at University of Cyprus.
2003 – 2008:	Special Scientist & Teaching Assistant at University of Cyprus.

Areas of Concentration/ Research Interests:
Digital Design CAD tools development. Very Large Scale Integration (VLSI) design, verification and testing. Design for Testability. High Quality digital circuit testing. Self-testing and fault tolerant architectures. Parallel algorithms for simulation and testing.

Professional Associations
***Organization/field*:** Institute of Electrical and Electronic Engineers (IEEE)
***Title*:** Full member, former secretary of IEEE Student Branch/University of Cyprus.
***Organization/field*:** Technical Chamber of Cyprus (ETEK)
***Title*:** Member.

Funding (grants, contracts, research awards)

- "Delay Testing for VLSI Circuits" funded by the Cyprus Research Promotion Foundation (IPE) under the Programme for the Support of Young Researchers (PENEK). **Amount**: £13,000 (€ 22,212) **Date:** 2004
- "Novel Methods for Fault Tolerant Systems-on-Chip (SoCs)" funded by the Intel Corporation. **Amount**: £15,000 (€ 25,630) **Date:** 2006

- "Automated Sonar-Thermal Monitoring for Sea Border Security", funded by Cyprus Research Promotion Foundation (IPE). Participated as a researcher. **Amount**: € 180.000 **Date:** 2012

Awards/Distinctions:

- Greek Government Scholarship Foundation (IKY–Hellas) scholarship for academic performance while being 2nd ranked undergraduate student.
- Graduate first among his class (distinction).
- Award from Greek Technical Chamber (TEE) for his overall academic performance.
- Cyprus Government Scholarship Foundation (IKY-Cyprus) scholarship for graduate studies.
- Best paper nomination for conference paper [2] under conference proceedings.
- Travel Grant for presenting the Doctoral Dissertation in PhD Forum at Design And Test in Europe (DATE) conference, Munich, 2008.

Languages: Greek (fluent), English (fluent), French (proficient), German (competent)

Research & Publications

Doctoral Dissertation: "High Quality Test Pattern Generation Techniques for Digital VLSI Circuits", University of Cyprus, Mar. 2009. (PhD Defense Jan 2009).

Books Edited, Written or Translated: ---

Chapters in Books:

[1] C. Bolchini, M. K. Michael, A. Miele, S. Neophytou "Dependability Threads", in M. Ottavi, S. Pontarelli, D. Gizopoulos, "Dependable Multicore Architectures at Nanoscale", 1st Ed., August 2017, Springer, ISBN-13: 9783319544212**.**

Monographs: ---

Journal Articles – in print or submitted for publication

[1] **S. N. Neophytou**, M. K. Michael, and S. Tragoudas, "Functions for Quality Transition-Fault Tests and Their Applications in Test-Set Enhancement", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 25, no. 12, pp. 3026–3035, Dec. 2006. *

[2] **S. Neophytou** and M. K. Michael, "Test Set Generation with a Large Number of Unspecified Bits Using Static and Dynamic Techniques", *IEEE Transactions on Computers* 59(3): 301-316, Mar. 2010. *

[3] **S. Neophytou** and M. K. Michael: "Test Pattern Generation of Relaxed *n*-Detect Test Sets", *IEEE Transactions on Very Large Scale Integration (VLSI)* Volume: 20 Issue:3, pp 410-423, March 2012. *

[4] **S. N. Neophytou**, Maria K. Michael, "A Non-Enumerative Technique for Measuring Path Correlation in Digital Circuits", *Journal of Electronic Testing: Theory and Application* (JETTA), 28(6), pp 843-856, Springer, Oct 2012. *

[5] **S. Neophytou** and M. K. Michael, "Multiple detection test generation with diversified fault partitioning paths", *Microprocessors and Microsystems – Embedded Hardware Design*, vol. 38, no. 6, pp. 585-597, Elsevier, Aug. 2014. *

[6] S. Hadjitheophanous, **S. N. Neophytou**, and M. K. Michael, "Exploiting Shared-Memory to Steer Scalability of Fault Simulation in Multicore Systems", submitted in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Nov. 2017.

*	Journals (refereed)	***	Electronic Journal
**	Invited papers	****	Non-refereed Journals

Bulletins or Reports: ---

Abstracts – in print or accepted: ---

Conference Proceedings:

[1] M. K. Michael, **S. Neophytou**, and S. Tragoudas, "Functions for Quality Transition Fault Tests", in *Proc. of IEEE International Symposium on Quality of Electronic Design*, pp. 327–332, 2005, San Jose, CA, USA.

[2] **S. Neophytou** and M. K. Michael and S. Tragoudas, "Test Set Enhancement for Quality Transition Faults using Function-based Methods", in *Proc. of the 15th IEEE/ACM Great Lakes Symposium on VLSI*, pp. 182–187, 2005, Chicago, IL, USA.

[3] **S. Neophytou**, M. K. Michael, and S. Tragoudas, "Efficient Deterministic Test Generation for BIST Schemes with LFSR Reseeding", *Proc. of IEEE International On-Line Testing Symposium*, pp. 43–50, 2006, Lake of Como, Italy.

[4] **S. Neophytou** and M. K. Michael, "Hierarchical Fault Compatibility Identification for Test Generation with a Small Number of Specified Bits", in *Proc. of IEEE Defect and Fault Tolerance Symposium*, pp. 439–447, Sep. 2007, Rome, Italy.

[5] **S. Neophytou** and M. K. Michael, "Two New Methods for Accurate Test Set Relaxation via Test Set Replacement", in *Proc. of IEEE International Symposium on Quality of Electronic Design*, pp. 827-831, Mar. 2008, San Jose, CA, USA.

[6] **S. Neophytou** and M. K. Michael, "On the Relaxation of N-detect Test Sets," in *Proc. of IEEE VLSI Test Symposium*, pp. 187-192, Apr. 2008, San Diego, CA, USA.

[7] **S. Neophytou**, M. K. Michael, K. Christou: "Generating Diverse Test Sets for Multiple Fault Detections Based on Fault Cone Partitioning". *in Proc. of IEEE Defect and Fault Tolerance Symposium*, pp. 401-409, Oct. 2009, Chicago, IL, USA.

[8] K. Christou, M. K. Michael, **S. Neophytou**: "Identification of Critical Primitive Path Delay Faults without any Path Enumeration", *in Proc. of IEEE VLSI Test Symposium*, pp 9-14, Apr. 2010, Santa Cruz, CA, USA.

[9] **S. Neophytou**, K. Christou, M. K. Michael: "An Approach for Quantifying Path Correlation in Digital Circuits without any Path or Segment Enumeration", *in Proc. of the IEEE European Test Symposium*, pp 141-146, May 2011, Trondheim, Norway.

[10] **S. Neophytou**, S. Hadjitheophanous, M. K. Michael: "On the Impact of Fault List Partitioning in Parallel Implementations for Dynamic Test Compaction Considering Multicore Systems" *in Proc. of the IEEE International Design and Test Symposium,* Dec. 2013, Marrakesh, Morocco.

[11] I. Voyiatzis, **S. Neophytou**, M. K. Michael, S. Hadjitheophanous, C. Sgouropoulou, C. Efstathiou: "Test Set Embedding into Accumulator-Generated Sequences Targeting

Hard-to-Detect Faults", *IEEE International Design and Test Symposium,* Dec. 2013, Marrakesh, Morocco.

[12] I. Kyriakides, **S. Neophytou**, A. Kounoudes, K. Michail, Y. Argyrou, T. Wieland, "Processing and Communications Rate Requirements in Sensor Networks for Physical Thread Assessment", in Proc. of *International Conference on Critical Information Infrastructures Security (CRITIS)*, Oct. 2014, Limassol, Cyprus.

[13] **S. Neophytou** and M. K. Michael, "Optimal variable ordering in ZBDD-based path representations for directed acyclic graphs". in Proc. of *IEEE International Conference on Computer Design (ICCD)*, pp. 489-492, Oct. 2014, Seoul, Korea.

[14] **S. Neophytou** and M. K. Michael, "Tackling the complexity of exact path delay fault grading for path intensive circuits". in Proc. of *IEEE Test Symposium (ETS)*, May. 2015, Cluj-Napoca, Romania.

[15] S. Hadjitheophanous, **S. Neophytou**, M. K. Michael: "Scalable Parallel Fault Simulation for Shared-Memory Multiprocessor Systems" in Proc. of *IEEE VLSI Test Symposium (VTS),* Apr. 2016, Las Vegas, USA.

[16] S. Hadjitheophanous, **S. Neophytou**, M. K. Michael: "Utilizing Shared Memory Multi-cores to Speed-up the ATPG process", in Proc. of *IEEE European Test Symposium (ETS),* May, 2016, Amsterdam, Netherlands.

Conference Presentations

Poster Sessions: Presented Doctoral Dissertation at Design And Test in Europe (DATE) Conference in Munich, 2008.

Round Table Discussions: ---

Symposium Presentation: Presented articles [4], [5], [7],[9], [10],[14] and [16] listed under conference proceedings.

Invited Speaker: "Sea-Border Security System", at *European Network of Law Enforcement Technology Service,* 19/09/12, Larnaca, Cyprus.

Other Scholarly Activities

Conference Organizing:

- Local Arrangements Chair of the European Test Symposium (ETS) 2017 held in Limassol on May 2017.
- Local member of the organising committee of the Test Spring School held in Nicosia on May 2017.

Editorial Boards: ---

Reviewer:

- IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems.
- IEEE Trans. on Computers.
- IEEE Trans. on Very Large Scale Integration (VLSI).
- IEEE Trans. on Emerging Topics of Computing.
- IEEE European Test Symposium (ETS).
- IEEE VLSI Test Symposium (VTS).

Collaborations: Kios Research Centre, University of Cyprus.

Committees:

- Member of Management Committee of the COST action IC1103 "*MEDIAN: Manufacturable and Dependable Multicore Architectures at Nanoscale*", representing Cyprus.
- Member of Management Committee of the COST action CA16222 "*Wider Impacts and Scenario Evaluation of Autonomous and Connected Transport*", representing Cyprus.
- Member of the Cyprus Research Promotion Foundation (IPE) advisory committee for Information and Communications Technology (ICT).
- Member of Technical Program Committee of European Test Symposium.
- Member of the Proposal Evaluation Committee for ICT, Greece. Committee formed by the General Secretarial of Research and Technology (ΓΓΕΤ), Greek Ministry of Education.

Proposals:

- Contributed in the preparation of 7 research project proposals to Cyprus RPF (IPE) since January 2009, more than 20 overall.
- Submitted a proposal to the UNIVERSITAS FOUNDATION'S SEED GRANT, 2016.

Experience

Administrative:

- Computer Engineering Programme Coordinator.
- Chair the Engineering Programmes Promotional Committee.
- Member of the Ad-hoc committee to refresh Electrical and Computer Engineering programmes.
- Member of the hiring committee for 3 full time faculty members (RTF).
- Member of the hiring committee for 8 part time faculty (visitors).
- Member of the School of Sciences and Engineering Council, 2013-2015.
- Contributed in the preparation of the Master's Degree in electrical Engineering offered by the department.
- Contributed in the preparation for the ECPU visit in 2010.
- Contributed in the preparation of the ECTS project for the courses I teach and as the Computer Engineering programme co-ordinator

Advisory:

- Supervised 15 BSc students for their final year projects.
- Supervise 4 BSc students for their final year projects.
- Member of the final year project committee for 25 BSc students
- Supervise 2 MSc Student.
- Member of the PhD defence committee of a PhD candidate at ECE Department, University of Cyprus.
- Co-supervise a PhD student at KIOS Research Centre, University of Cyprus.

Teaching: (seminars designed, courses taught)

As a Teaching Assistant

- Introduction to Technology Laboratory
- Operating Systems Laboratory
- Digital Logic Design

- Digital Logic Design Laboratory
- Circuits and Measurements Laboratory
- Computer Organization and Microprocessors
- Computer Organization and Microprocessors Laboratory
- Computer Aided Design for VLSI design Laboratory

As an Instructor

- Network Analysis Laboratory
- Introduction to VLSI Design
- Digital Systems
- Microprocessor Interfacing
- Digital System's Laboratory
- Electronics II
- Digital Integrated Circuits
- Programming for Engineers
- Advanced Computer Architecture
- VLSI Testing and Diagnosis for VLSI Systems
- Embedded Systems
- Senior Year Project.